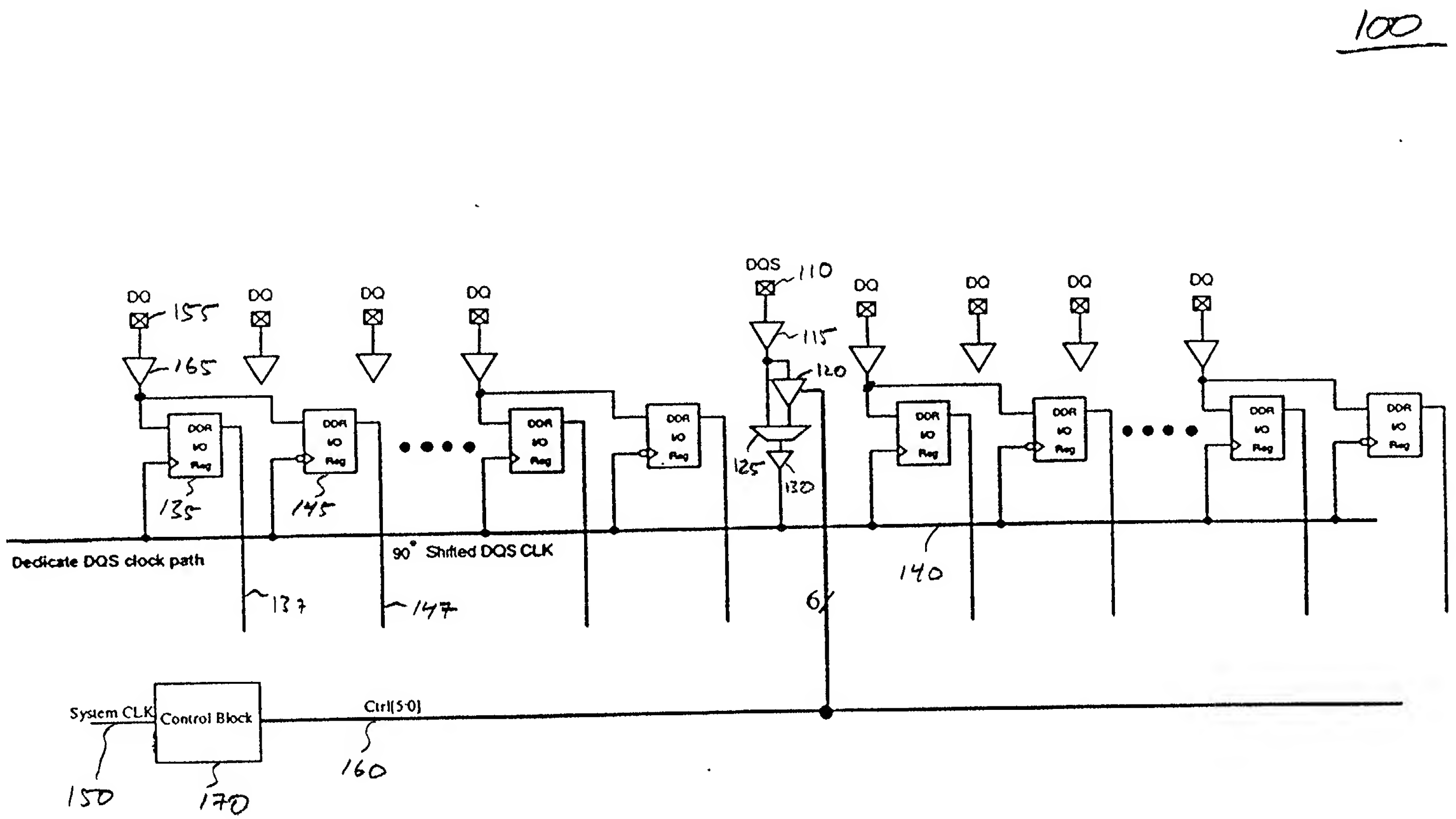

100
DQ
155
165
DQ
DQ
DQ
DQS
110
115
120
DQ
DQ
DQ
DQ
DDR
I/O
Reg
135
145
125
130
Dedicate DQS clock path
90° Shifted DQS CLK
137
147
6
140
System CLK
Control Block
Ctrl[5:0]
150
170
160

FIGURE 1

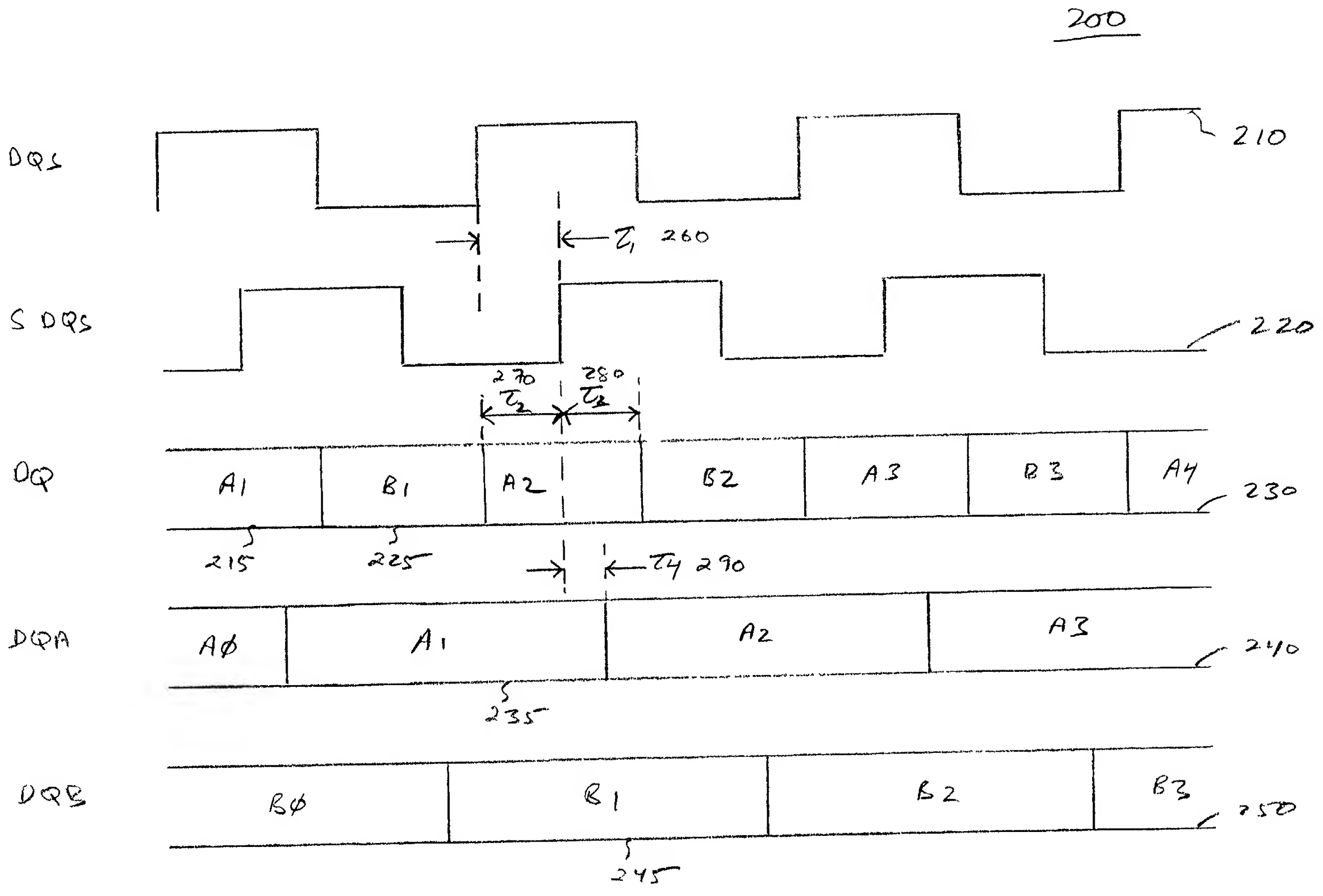

200
DQS
SDQS
DQ
DQA
DQB
210
220
230
240
250
τ_1 260
270 τ_2
280 τ_3
τ_4 290
A1
B1
A2
B2
A3
B3
A4
215
225
A0
A1
A2
A3
235
B0
B1
B2
B3
245

Figure 2

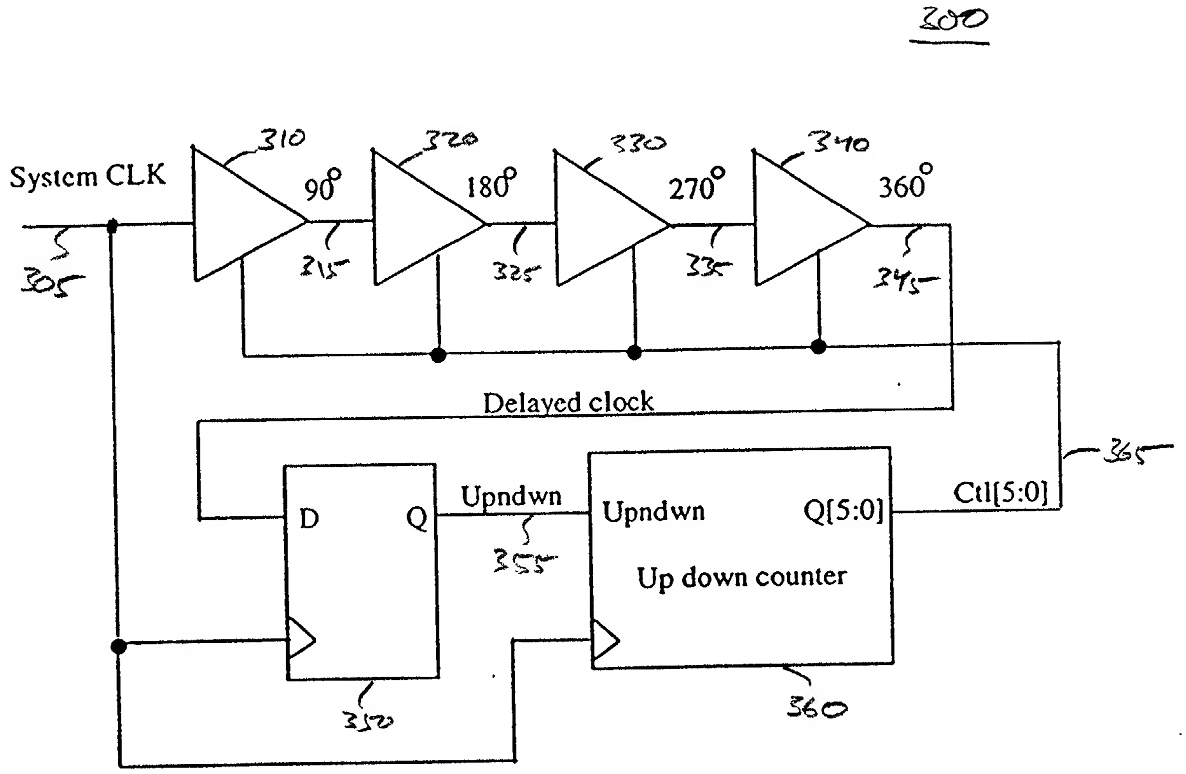

300
System CLK
305
310
320
330
340
90°
180°
270°
360°
315
325
335
345
Delayed clock
D
Q
Upndwn
355
350
Upndwn
Q[5:0]
Up down counter
360
Ctl[5:0]
365

FIGURE 3

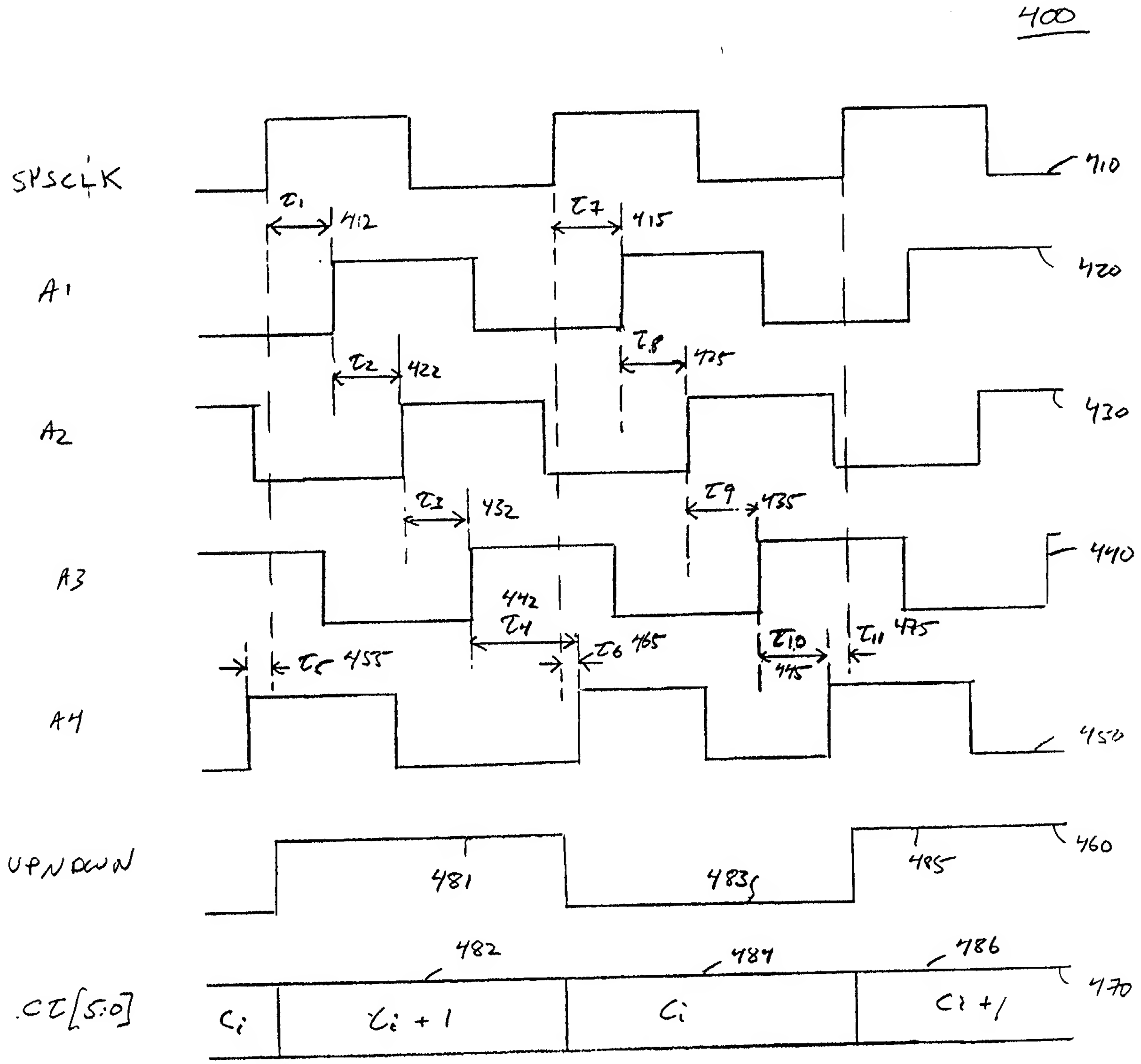

400
SYSCLK
A1
A2
A3
A4
UPNDOWN
CT[5:0]
410
420
430
440
450
460
470
τ1
412
τ7
415
τ2
422
τ8
425
τ3
432
τ9
435
442
τ4
τ5
455
τ6
465
τ10
445
τ11
475
481
483
485
482
484
486
Ci
Ci + 1
Ci
Ci +1

FIGURE 4

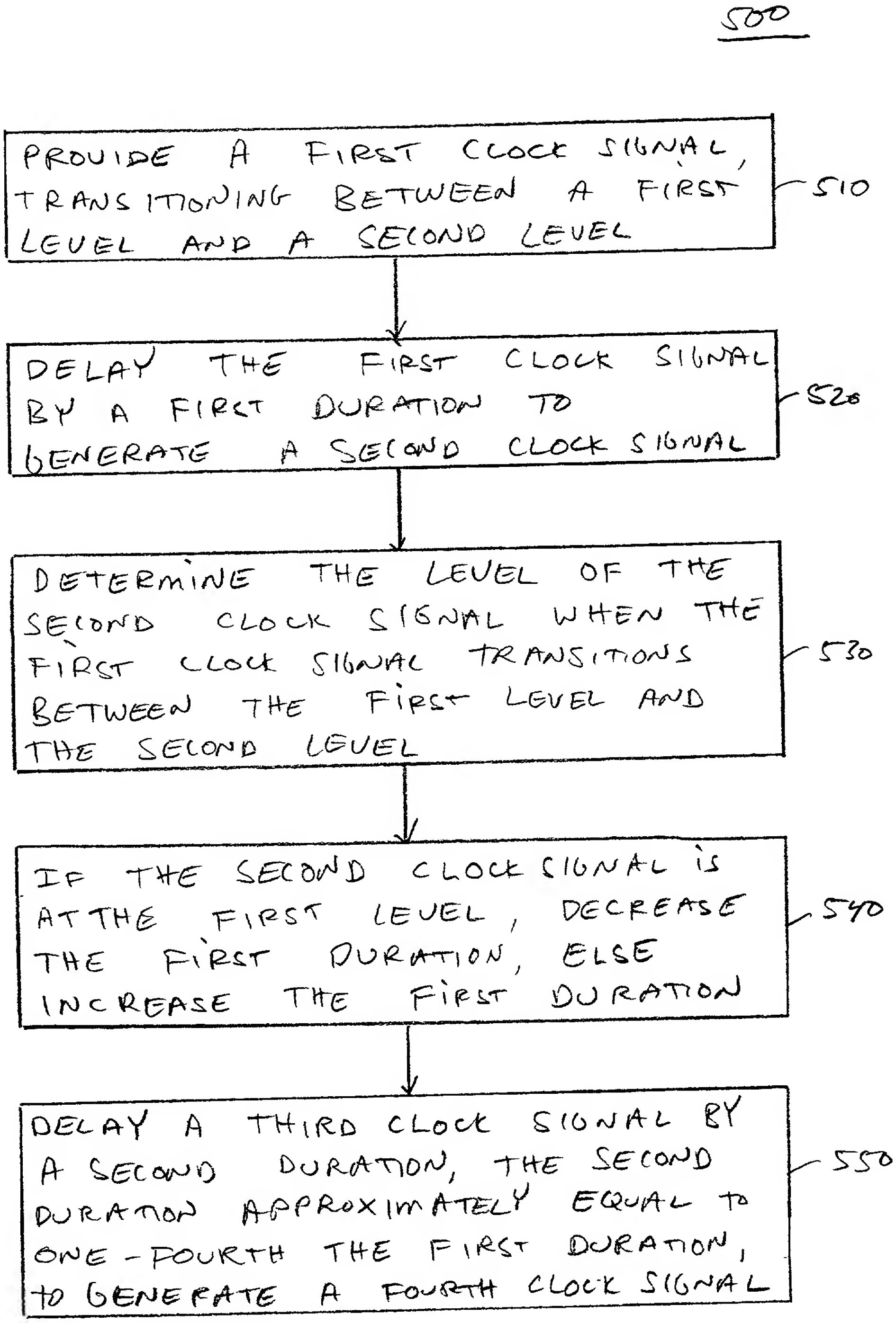

500
PROVIDE A FIRST CLOCK SIGNAL, TRANSITIONING BETWEEN A FIRST LEVEL AND A SECOND LEVEL
510
DELAY THE FIRST CLOCK SIGNAL BY A FIRST DURATION TO GENERATE A SECOND CLOCK SIGNAL
520
DETERMINE THE LEVEL OF THE SECOND CLOCK SIGNAL WHEN THE FIRST CLOCK SIGNAL TRANSITIONS BETWEEN THE FIRST LEVEL AND THE SECOND LEVEL
530
IF THE SECOND CLOCK SIGNAL IS AT THE FIRST LEVEL, DECREASE THE FIRST DURATION, ELSE INCREASE THE FIRST DURATION
540
DELAY A THIRD CLOCK SIGNAL BY A SECOND DURATION, THE SECOND DURATION APPROXIMATELY EQUAL TO ONE-FOURTH THE FIRST DURATION, TO GENERATE A FOURTH CLOCK SIGNAL
550

FIGURE 5

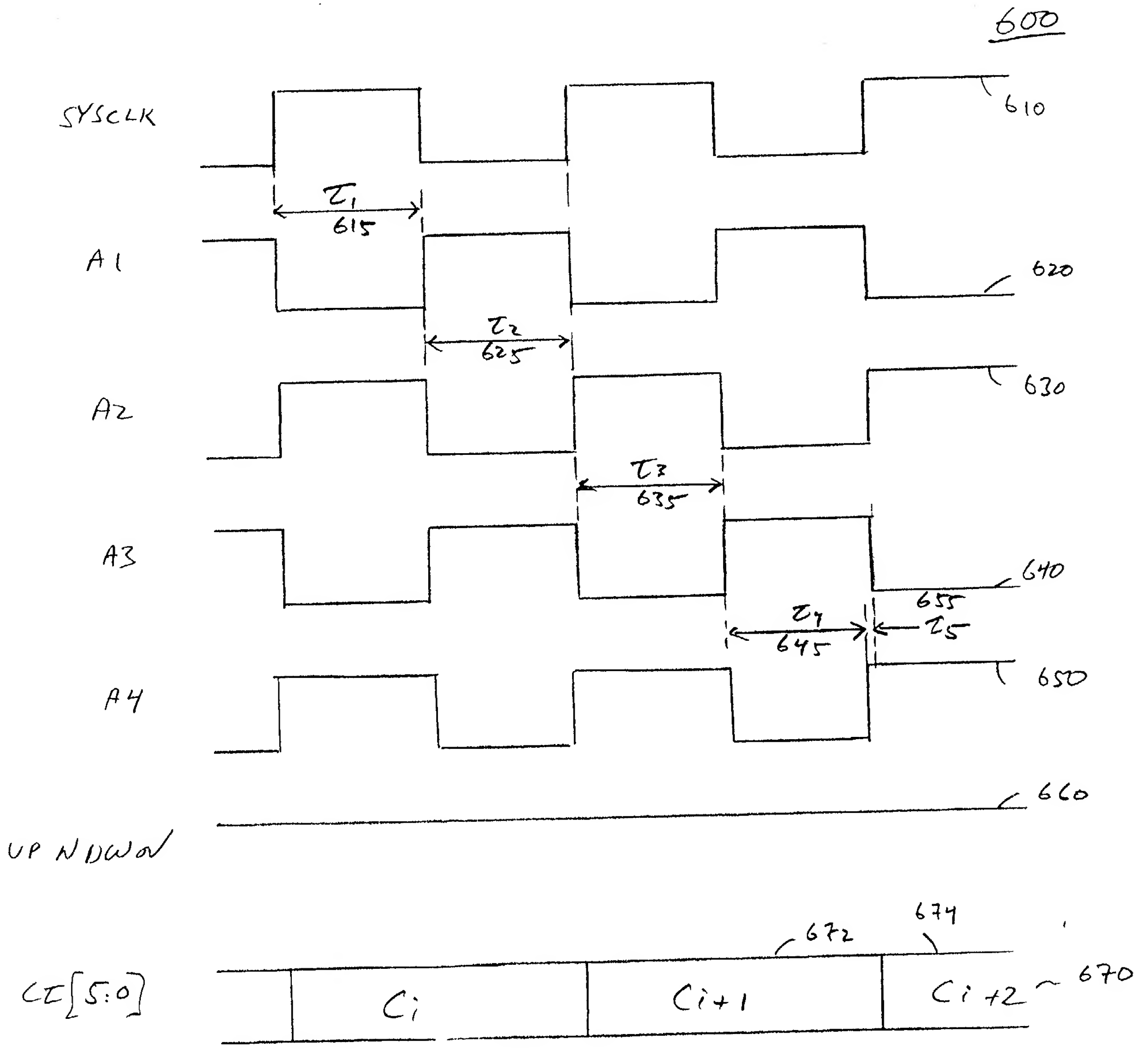

600
SYSCLK
A1
A2
A3
A4
UP NDWN
CI[5:0]
610
620
630
640
650
660
670
672
674
τ_1 615
τ_2 625
τ_3 635
τ_4 645
τ_5 655
Ci
Ci+1
Ci+2

FIGURE 6

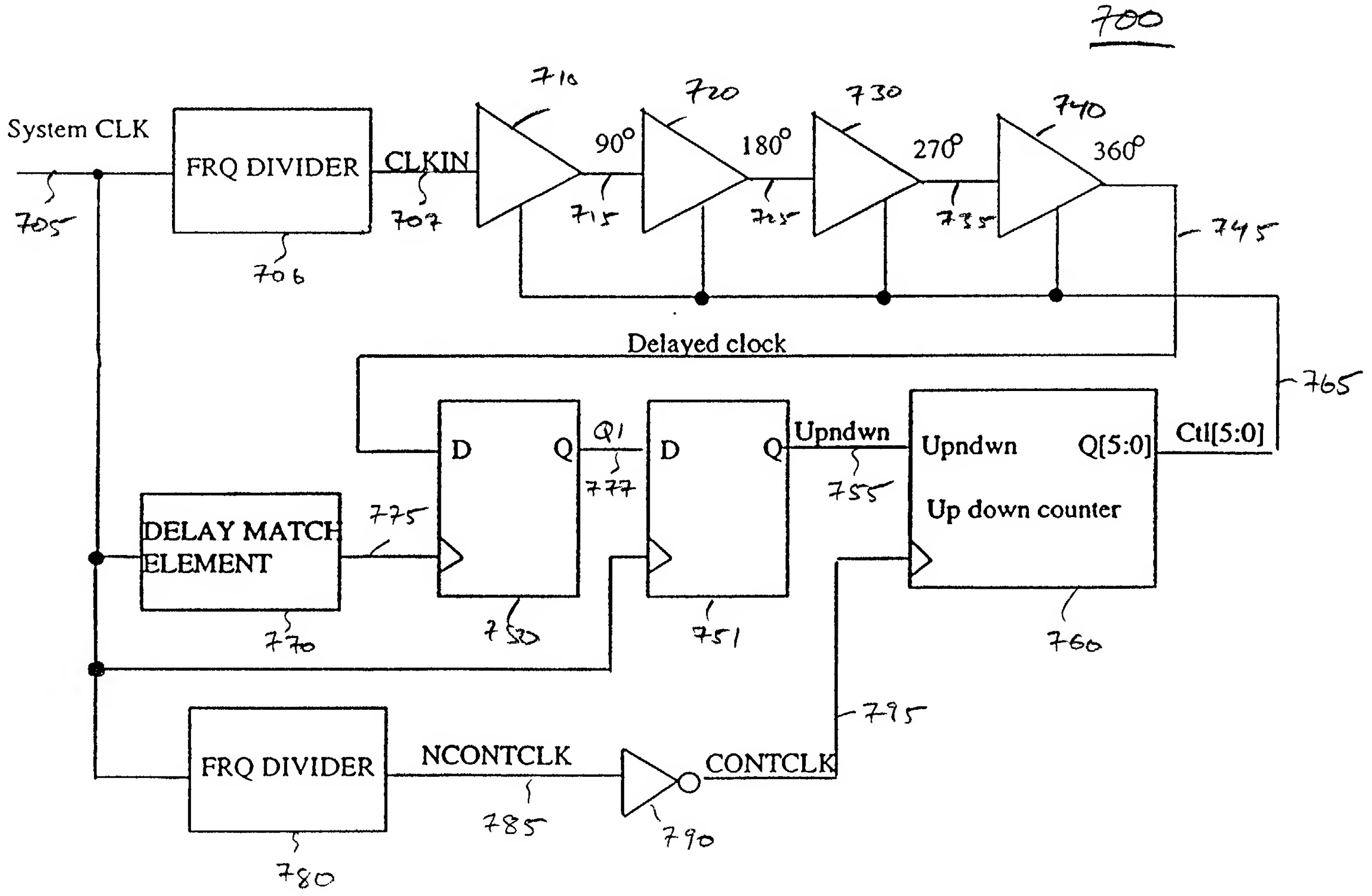

700
System CLK
705
FRQ DIVIDER
706
CLKIN
707
710
90°
715
720
180°
725
730
270°
735
740
360°
745
Delayed clock
765
D
Q
Q1
777
D
Q
Upndwn
755
Upndwn
Q[5:0]
Up down counter
Ctl[5:0]
DELAY MATCH ELEMENT
770
775
750
751
760
795
FRQ DIVIDER
780
NCONTCLK
785
790
CONTCLK

FIGURE 7

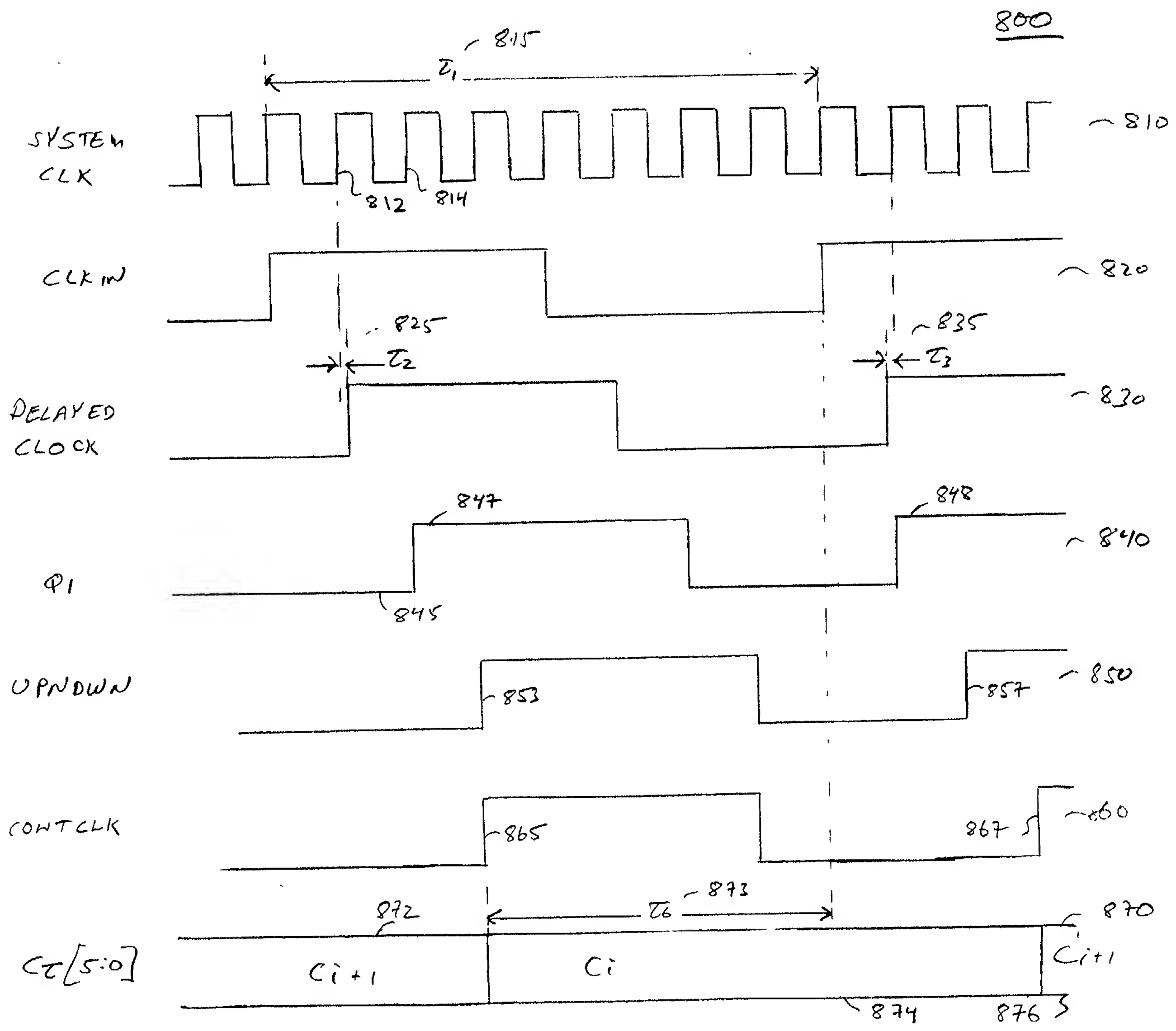

800
τ_1
815
SYSTEM CLK
810
812
814
CLK IN
820
825
τ_2
835
τ_3
DELAYED CLOCK
830
847
848
Q1
840
845
UPNDWN
853
857
850
CONTCLK
865
867
860
872
τ_6
873
870
CT[5:0]
Ci+1
Ci
Ci+1
874
876

FIGURE 8

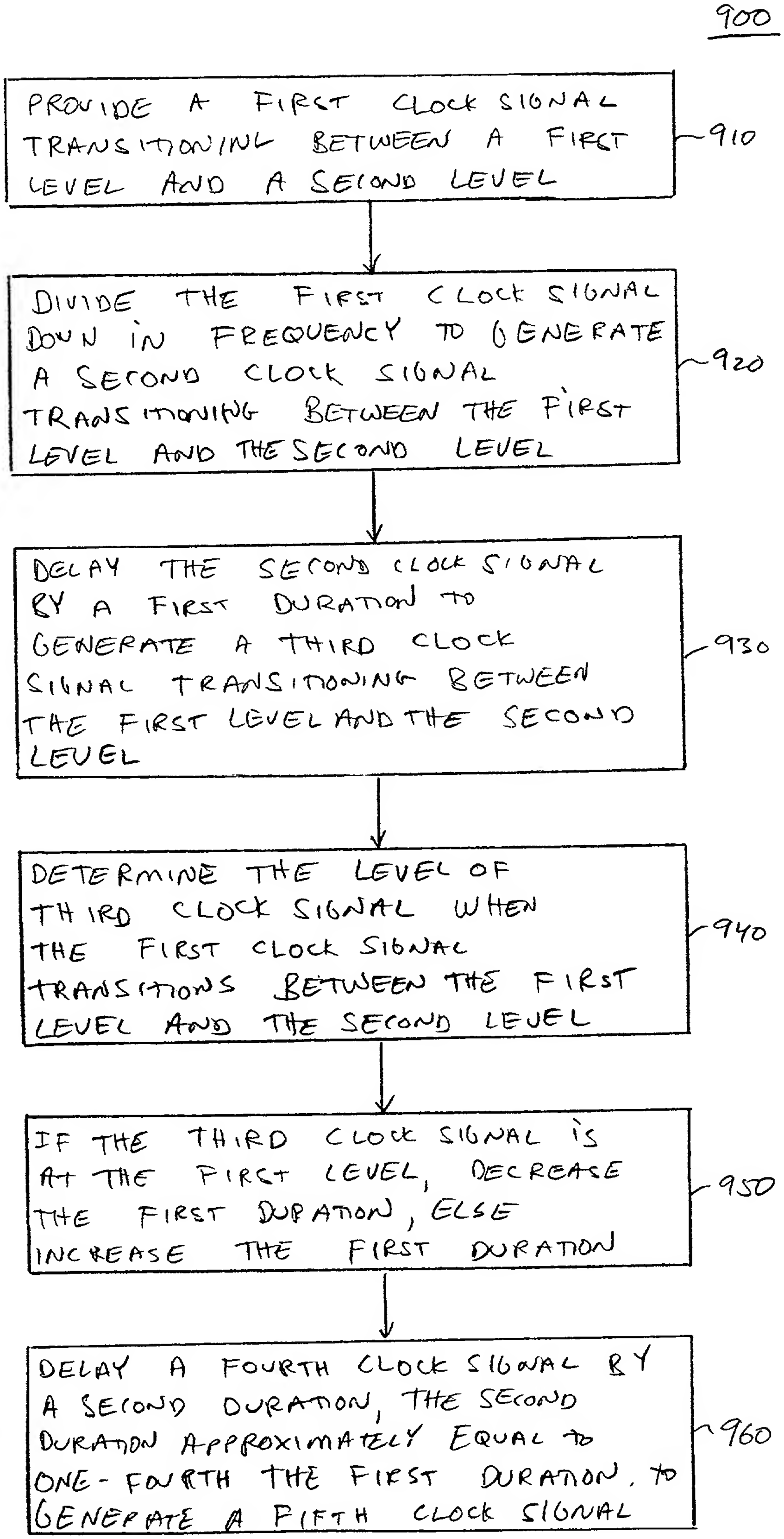

900
PROVIDE A FIRST CLOCK SIGNAL TRANSITIONING BETWEEN A FIRST LEVEL AND A SECOND LEVEL
910
DIVIDE THE FIRST CLOCK SIGNAL DOWN IN FREQUENCY TO GENERATE A SECOND CLOCK SIGNAL TRANSITIONING BETWEEN THE FIRST LEVEL AND THE SECOND LEVEL
920
DELAY THE SECOND CLOCK SIGNAL BY A FIRST DURATION TO GENERATE A THIRD CLOCK SIGNAL TRANSITIONING BETWEEN THE FIRST LEVEL AND THE SECOND LEVEL
930
DETERMINE THE LEVEL OF THIRD CLOCK SIGNAL WHEN THE FIRST CLOCK SIGNAL TRANSITIONS BETWEEN THE FIRST LEVEL AND THE SECOND LEVEL
940
IF THE THIRD CLOCK SIGNAL IS AT THE FIRST LEVEL, DECREASE THE FIRST DURATION, ELSE INCREASE THE FIRST DURATION
950
DELAY A FOURTH CLOCK SIGNAL BY A SECOND DURATION, THE SECOND DURATION APPROXIMATELY EQUAL TO ONE-FOURTH THE FIRST DURATION, TO GENERATE A FIFTH CLOCK SIGNAL
960

FIGURE 9

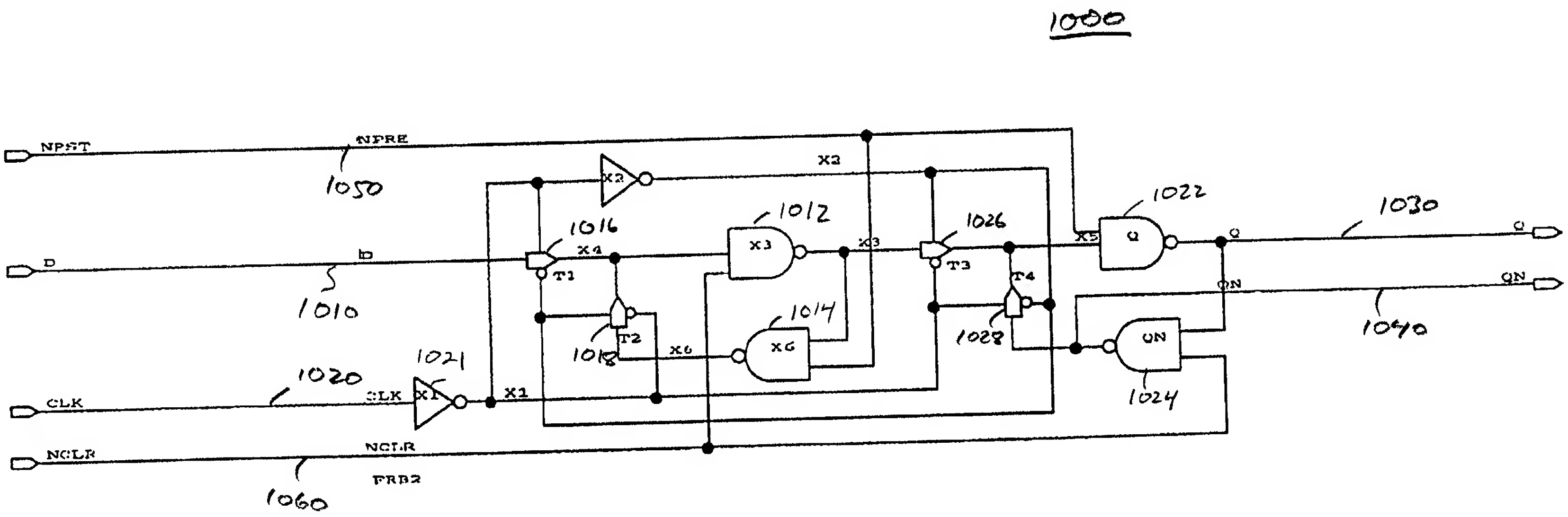

1000
NPST
NPRE
1050
X2
D
D
1010
1016
X4
T1
1012
X3
X3
1014
X6
X6
1018
T2
1026
T3
T4
1028
X5
Q
1022
Q
1030
Q
QN
QN
1024
QN
1040
CLK
1020
CLK
X1
1021
X1
NCLR
NCLR
1060
PRB2

Figure 10

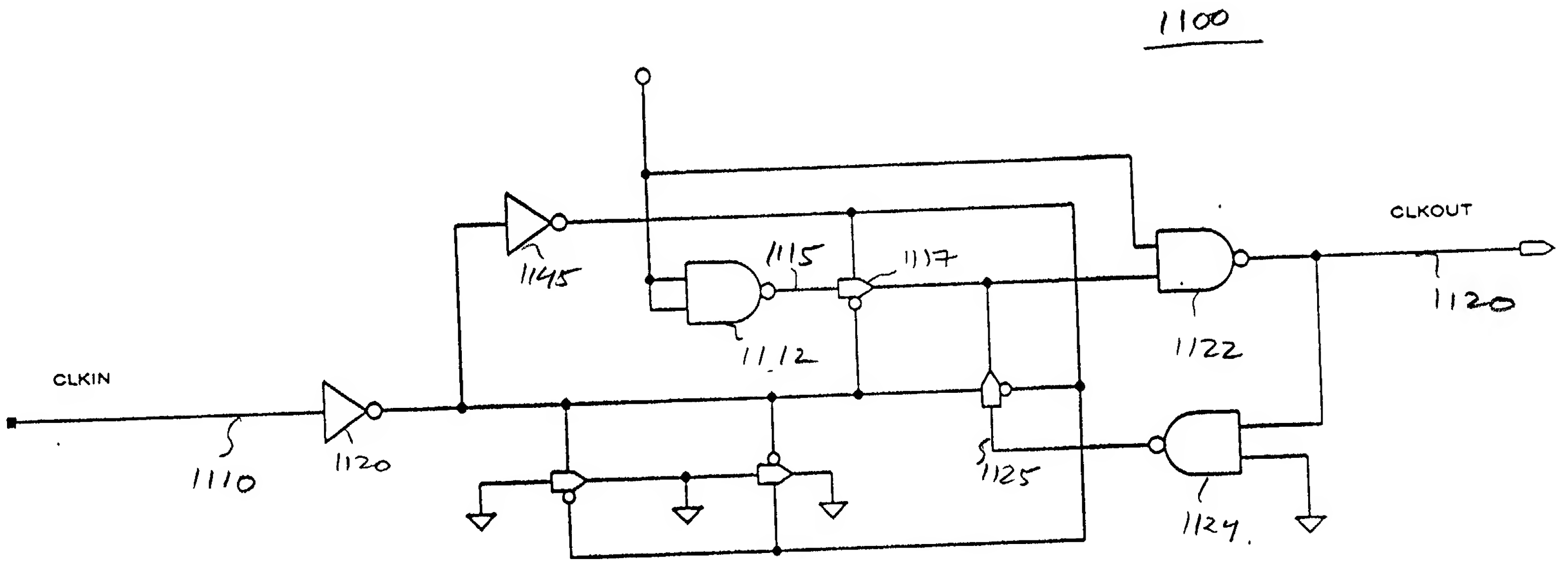

1100
CLKIN
1110
1120
1145
1115
1117
11.12
1122
1125
1124
CLKOUT
1120

FIGURE 11

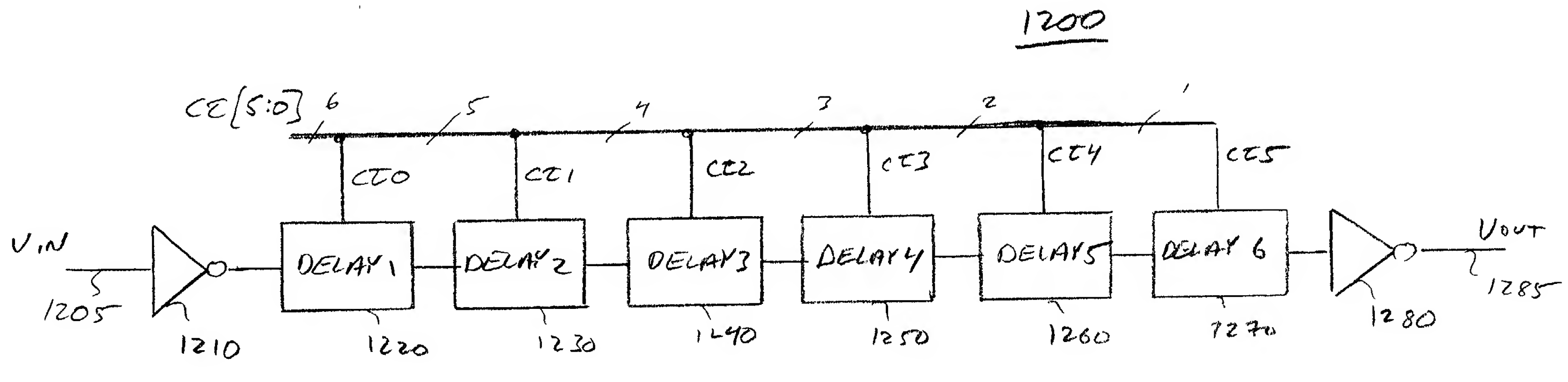

1200
CE[5:0]
6
5
4
3
2
1
CE0
CE1
CE2
CE3
CE4
CE5
VIN
1205
1210
DELAY 1
1220
DELAY 2
1230
DELAY 3
1240
DELAY 4
1250
DELAY 5
1260
DELAY 6
1270
1280
VOUT
1285

FIGURE 12

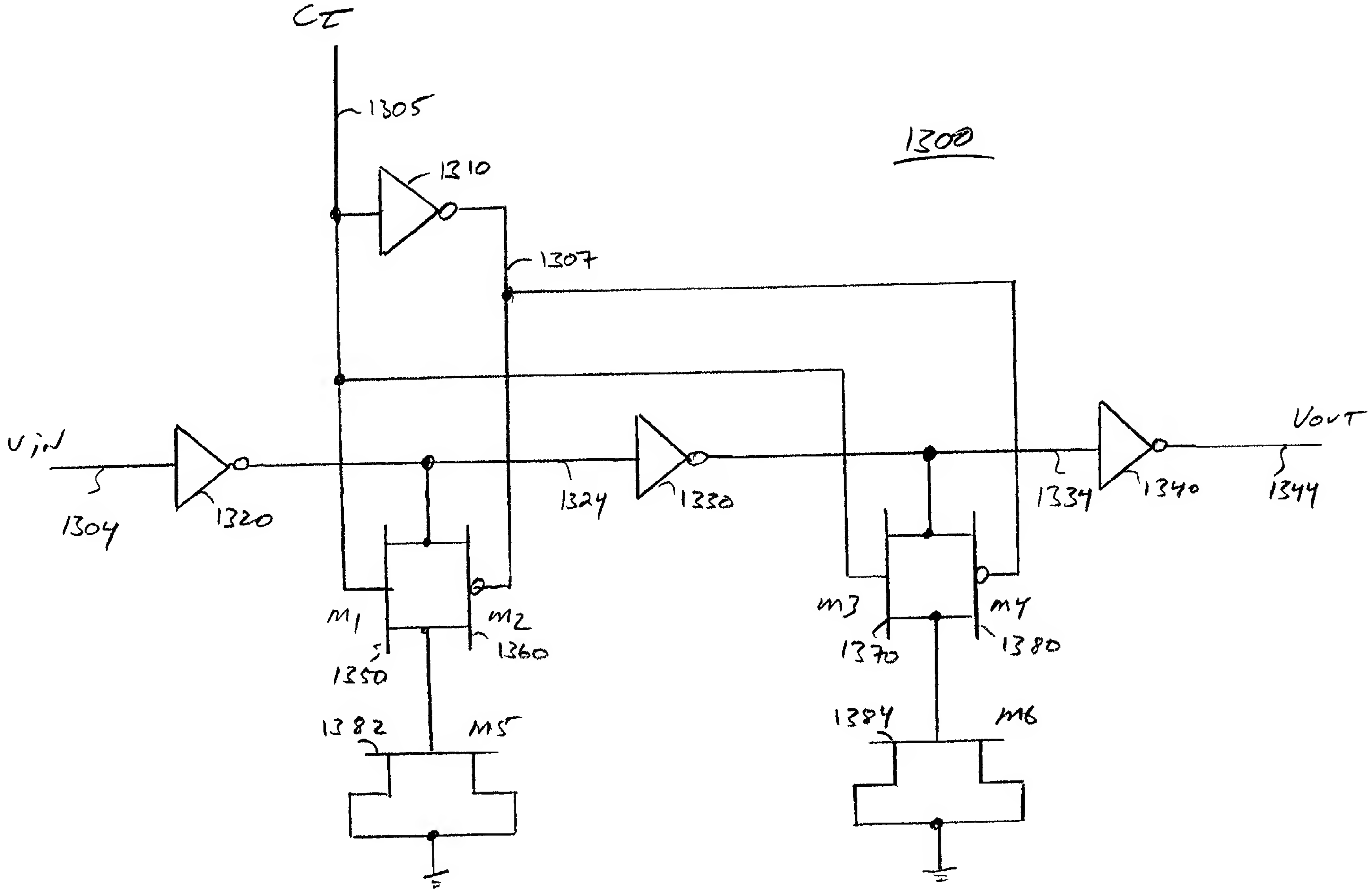

CT
1305
1310
1307
1300
Vin
1304
1320
1324
1330
1334
1340
Vout
1344
M1
1350
M2
1360
M3
1370
M4
1380
1382
M5
1384
M6

FIGURE 13

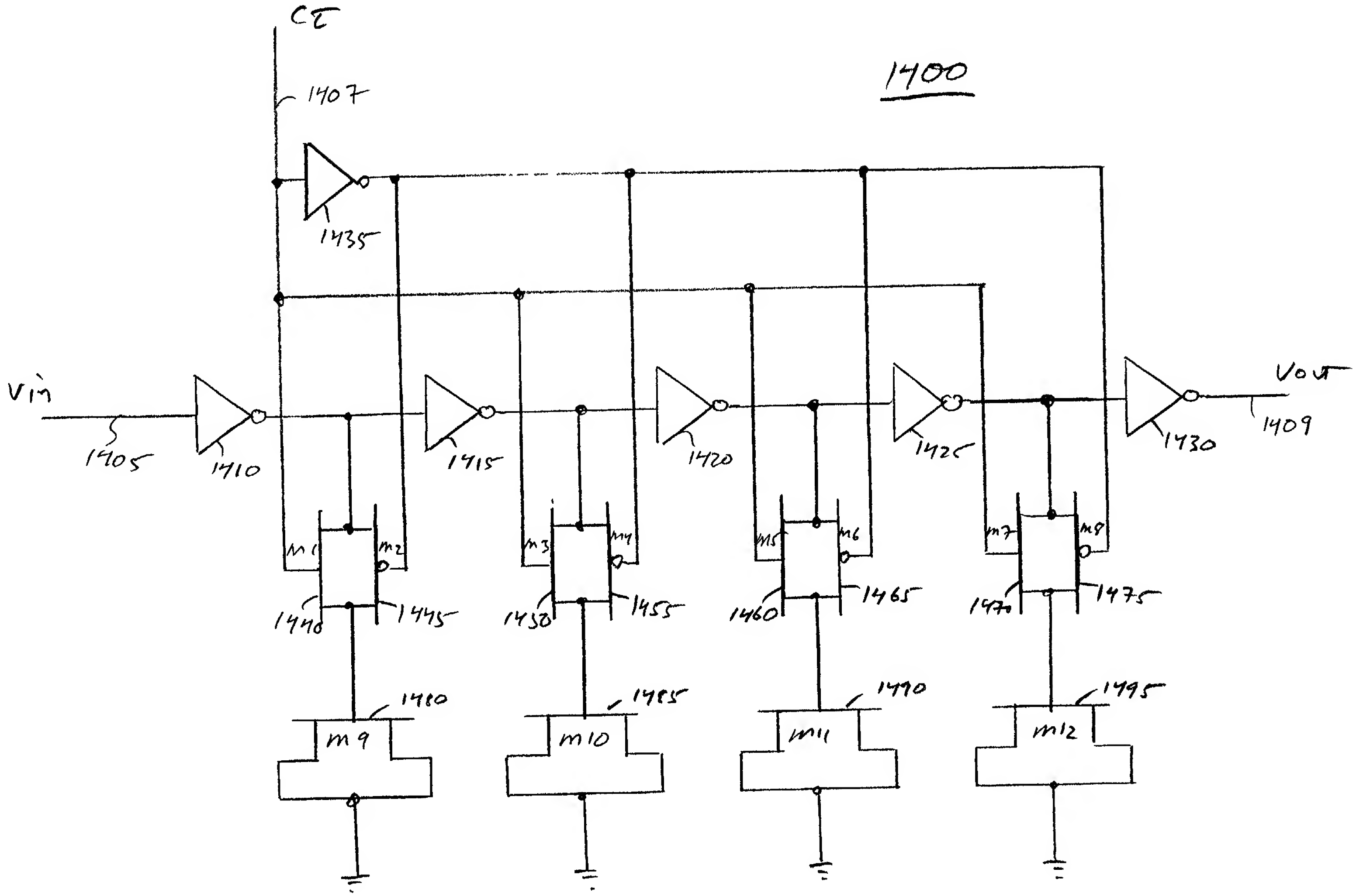
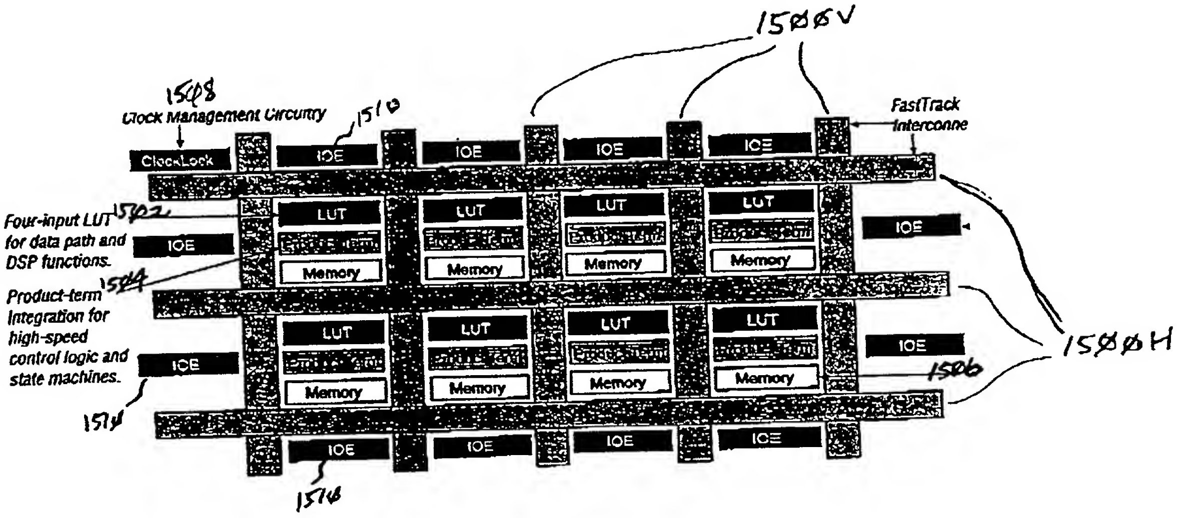
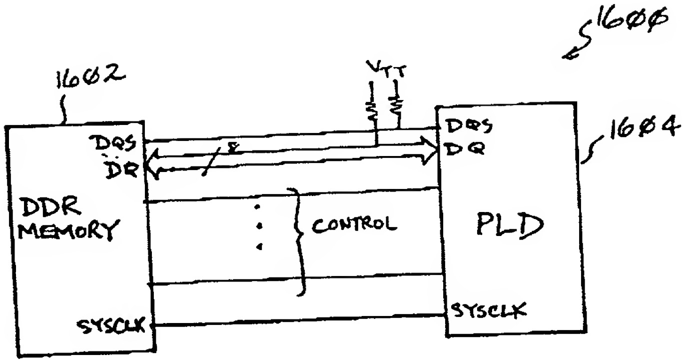

CE
1407
1400
1435
Vin
1405
1410
1415
1420
1425
1430
Vout
1409
m1
m2
m3
m4
m5
m6
m7
m8
1440
1445
1450
1455
1460
1465
1470
1475
1480
1485
1490
1495
m9
m10
m11
m12

FIGURE 14



- FIGURE 15 -



- FIGURE 16 -